IN THE SPECIFICATION

Please amend the paragraph beginning on page 8, line 3 as follows:

--The processing circuit [[1]] 101 shown in FIG. 1 can achieve a reduction of size and increase of speed by designing it like the processing circuit 201 using the processing circuit modules il_j (j is integer of 2 or more) combining the processings $C_{i,1}$ to $C_{i,1i}$ in the processing circuit modules as shown in FIG. 2.--